47P.

FINAL REPORT

Contract NAS8-5472

ANALOG-TO-DIGITAL CONVERTER
for
HIGH ACCURACY, SEVERE ENVIRONMENT OPERATION

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P. A. Tone
W. R. Brown, III
J. M. Walter

Aerospace Systems
Dynatronics, Inc.
Orlando, Florida

April 1964

Prepared for

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama

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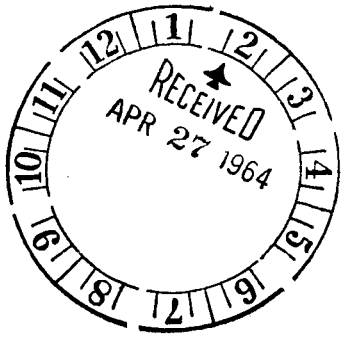

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FOREWORD

The work described herein was accomplished by the authors under NASA-MSFC Contract NAS8-5472, within the Aerospace Systems section at Dynatronics, Inc. Contract technical representatives at NASA-MSFC were Messrs. W. O. Frost and C. D. Smith. Acceptance testing of the Prototype (breadboard) unit and environmental testing of the Evaluation (final) unit were jointly performed by Dynatronics, Inc. and NASA-MSFC engineering personnel at the NASA-MSFC Astrionics Laboratory.

This report is not classified.

ABSTRACT

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The many considerations evolving a design approach for a highly accurate (0.05%, exclusive of quantizing error) high-speed analog-to-digital converter which exhibits this accuracy under severe environments (e.g., 105°C temperature range) are discussed. Accuracy, reliability, power consumption, and encoding rate are among these considerations. Types of errors typically encountered in successive-approximation encoding and their antidotes are discussed.

An innovation referred to as "variable-speed encoding" and an analysis revealing its advantage in minimizing overall encoding time while providing maximum accuracy, is presented. A detailed description and performance characteristics are given for the analog-to-digital converter (ADC) developed following these design principles. A design discussion of automatic zero and full-scale calibration circuits is included for possible future application, although these circuits were not included in the present ADC because of system considerations.

Finally, conclusions and recommendations resulting from the development program are offered.

Author:

1.0 INTRODUCTION

The "PCM telemetry era" was ushered in less than a decade ago, when an analog-to-digital converter was first employed as an important element of an operational airborne, time-division-multiplexing telemetry system to permit a vast improvement in attainable accuracies through the use of frequency-shift-keying techniques in the radio link. The "PCM bandwagon" has gathered additional momentum more recently due to the popularity (and indeed, necessity) of digital data handling techniques in ground processing equipment.

As transducers, signal conditioners, and multiplexing equipment have been improved, so have analog-to-digital converters (encoders). The "half-split" or "successive-approximation" technique has been highly developed and represents the present extent of the art as far as accuracy is concerned. However, the technique is by no means a completed art. That is, no fundamental limitation has been encountered to date which confounds attempts to further improve the accuracy of a successive-approximation type encoder (such as Johnson noise, for example, which limits the low-level performance of an amplifier). However, the types of errors encountered in this type encoder are often difficult to describe owing to its servo-loop type operation in which "causes" and "effects" cannot easily be distinguished. Inclusion of a non-linear element, the digital-to-analog converter, in this servo-loop makes the problem of defining errors (by measurement, as well as by analysis) even more formidable. Of course, the requirement for 0.1% absolute accuracy or better under the severe environment presented by a large space vehicle introduces many difficulties over those encountered in ground-based encoders.

It is the intent of this document to record the design approaches followed on development contract NAS8-5472. In addition, the types of errors anticipated and observed are described, and means of eliminating or reducing them are discussed. The unit itself is then described, along with an automatic zero and full-scale calibration technique. The conclusions and recommendations given include easily-realizable improvements to the existing design, as well as long-range suggestions.

2.0 DESIGN APPROACH

2.1 Design Goals

The design approach taken is best introduced by listing the design goals set forth at the beginning of the development effort. The several compromises involving these goals will then be considered.

1. Number of Bits: 10
2. Conversion Speed: 22 kc word rate minimum
3. Accuracy: 0.05% absolute (excluding quantizing error), $-20^{\circ}C$ to $+85^{\circ}C$
4. Input Level: 0 to +5 volts
5. Input Impedance: 1 megohm minimum
6. Outputs: Parallel only, stored until next word
7. Environment for 0.05% accuracy:
   - A. Temperature: $-20^{\circ}C$ to $+85^{\circ}C$
   - B. Humidity: 95% @ $50^{\circ}C$
   - C. Vibration: 20g, 20 to 2,000 cps
   - D. Shock: 100g, 11 millisec
   - E. Acceleration: $\pm$70g
   - F. Altitude: Deep Space
8. Power: +28 $\pm$ 4.2v dc with 3v peak-to-peak random noise superimposed, 8 watts, isolated supply
9. Reliability: 10,000 hours MTBF

10. Construction: Printed boards for analog and special-purpose logic circuits; welded modules for redundant logic circuits

The 10-bit capability was desired to provide a highly-accurate means of evaluating the readiness of the vehicle's measuring system itself, during prelaunch checkout. It represents a 4:1 reduction in peak quantizing error over that of more commonly used 8-bit encoders. A $\pm$ ½ bit quantizing error is about $\pm$ 0.05% for a 10-bit encoder, and makes a negligible contribution to system error, so additional bits could hardly be justified considering the data capacity tradeoff. Furthermore, the problems encountered in matching the 10-bit capability with $\pm$ 0.05% peak analog error are severe indeed.

The conversion speed was chosen to allow use of the ADC at system word rates as high as 14.4 kc. Asynchronous operation and stored parallel readout were required to allow simple interlace of ADC words with other digital words in parallel form (guidance computer, radar altimeter, synchronization patterns, etc.). An analog accuracy of $\pm$ 0.05% (due to drift, noise and ADC dynamic errors) would allow ADC error to be neglected during data reduction.

The environment is that anticipated in large space vehicles. The reliability goal of 10,000 hours MTBF is a 25% improvement over that of a previous ADC design. The hybrid construction approach was chosen to reduce the physical size and improve reliability of logic circuits while leaving analog circuits repairable. Also, it was anticipated that some temperature compensation of critical analog circuits would be required during manufacture.

Of all design goals, reliability was given greatest emphasis. (Accuracy ran a close second.) Redundancy techniques were not considered for this application because of the sacrifice in accuracy, or simplicity, or both. Instead, all circuitry was kept as simple as possible to reduce the total component count in the ADC. Also, worst-case design techniques were followed in logic circuits. All components were power-or-voltage derated as much as possible. Finally, temperature testing 15°C above and below the operating extremes of -20°C and +85°C was accomplished to "de-bug" the design.

2.2 Design Tradeoffs

The most basic design tradeoff in a successive-approximation ADC is that of speed vs accuracy. This tradeoff arises because of limited response in the comparator amplifier and reference supply, and its effect on the accuracy with which decisions on individual bits are made. The situation is further complicated by the low power requirement, since low power consumption results in high impedance levels, which in turn result in poor response. The desired conversion speed (sample rate) of 22 kc places the ADC well within the "high speed" category (1 kc to 100 kc conversion rate), but several ground based ADC's better this somewhat. That is, the requirement appears to be well within the state-of-the-art. However, various parallel decision techniques and low-impedance level operation are employed to overcome the comparator response problem in ground based ADC's and these approaches are generally undesirable for a high-reliability design because of the additional circuitry required. For example, at least one additional comparator amplifier would be required to implement the parallel technique. Low-impedance comparator operation improves response but requires an input buffer amplifier to achieve high input impedance. The input buffer would be another source of drift and noise, would reduce the ADC reliability somewhat, and would increase power consumption.

Another solution to the comparator response problem exists. Previous ADC designs have failed to fully take account of the amplitude dependence on the accuracy of individual bit decisions in addition to the response dependence. This is a very simple idea which is best explained by example. The most significant bit of a half-split ADC has a weight of $2^9/2^{10} = 512/1024$, or a 50% effect on the final output code. The least significant bit has a weight of only $2^0/2^{10} = 1/1024$, or only about a 0.1% effect on the code. It is obvious that any error source affecting the decision accuracy would have a much more drastic effect on the output code when applied to the most significant bit than when applied to the least significant bit. In fact, the same inaccuracy would produce a 512 times greater error for the MSB than for the LSB. (This is the reason ladder network resistors must be most precise in the most significant bits.)

Now, suppose one can design the comparator amplifier with a response independent of the input signal amplitude (e.g., does

not saturate for signals of any amplitude, since saturation causes transistor charge storage effects to have a dominant effect on amplifier response). Then comparator rise time or recovery time for a step function such as generated by the d-a converter is a constant, independent of the bit position. With this condition it should be possible to predict errors very accurately, knowing only the comparator response and ADC bit rate. More important, if ADC bit rate can be made variable, it should be possible to tailor bit settling times to comparator response in order to maximize the equivalent input accuracy with which each bit decision is made.

The use of an asynchronous sequencing technique makes it possible to provide settling times of any necessary duration, but limited in resolution by the ADC clock pulse spacing. The development effort culminating in the ADC-4 deliberately exploited this technique, referred to as "variable-speed encoding", as a solution to the comparator response problem.

The advantage of variable speed encoding can be seen easily. Suppose, for example, that a settling time of at least 6 μsec is needed for a 10-bit ADC's most significant bit. Then, as is customary, other bits would also be allowed 6 μsec. In this case the total encoding time would be 60 μsec (neglecting delays, etc.). However, as will be shown, it is possible to realize comparable performance using bit settling times of 6,6,4,4,4, 4,4,2,2,2 μsec for the 2^9 through 2^0 bits, respectively. The total encoding time for this case is only 38 μsec. The former ADC would be limited to conversion rates approaching 17 kc, while the latter one could encode at 26 kc with equal accuracy. The two ADC's differ only in their sequencing circuitry. The latter requires one additional flip-flop in the 2:1 counter string used, and a rearrangement of matrix diodes to detect the proper count conditions. Except for the additional flip-flop and 10 matrix diodes, the latter method has no greater component count. Its reliability is therefore reduced only slightly, much less than would result from use of parallel encoding techniques or an input buffer amplifier. Of course, variable-speed encoding can be employed only with asynchronous, parallel-storage ADC's which is an inherent limitation.

The settling time required for each bit can be very precisely predicted by a simple calculation. Comparator response, ADC

clock rate, and the number of counter stages in the ADC sequencer must also be known, or be arbitrary. It is useful to derive the relationship between sine wave response and step response for an RC low-pass network. Its 3 db point is

$$f_{3db} = \frac{1}{2\pi RC} = \frac{1}{T}$$

Solving the above relationship for the RC product,

$$RC \simeq .16T$$

This relates the sine wave <u>period</u> at the 3 db point to the RC <u>time constant</u> (rise time to 63% of final value). Since a linear amplifier approximates the roll-off characteristics of a lumped RC network, this relationship can be used to calculate the settling time of an amplifier whose sine wave response is known. This is a convenient procedure to follow because sine wave amplitudes are much more easily measured than pulse rise or fall times.

Table Ia tabulates calculated values of settling time errors vs settling times of 2, 4, 6, and 8 μsec. Here the comparator 3 db point is 160 kc, so

$$RC \simeq .16 \times \frac{1}{.16 \times 10^6} \simeq 1 \ \mu sec$$

"Arbitrary settling times" given in Table Ib are determined by placing a limit of .05% on the "error referred to the input" due to any one bit. Errors are determined by the following procedure.

1. Select an arbitrary settling time for the bit in question

2. Use the corresponding $(E/E_f) \times 100\%$ from Table Ia, taking the product of this and the bit contribution at the input as the error

3. If the result exceeds the error criterion (0.05%) choose the next longer settling time. If the result is much less than the error criterion, recalculate it using the next shorter settling time

Table I was calculated around a preliminary comparator design having a 160 kc bandwidth. Table II was then calculated using a 0.01% maximum error criterion, on the assumption that the bandwidth could be improved to 300 kc, and 300 kc comparator response was adopted as a design goal. Data on the completed ADC design, using settling times from Table II, shows that the 2^2 bit is indeed a worst-case for the ADC. The 2^7 bit appears to be a close runner-up, although these minute errors are difficult to observe. Errors involving 2^2 and 2^7 bits become appreciable at higher ADC clock rates, however, which experimentally substantiates the calculations.

It should be reiterated that this analysis will be most fruitful only when the comparator amplifier has a response that does not worsen for large-amplitude signals. As is discussed in the equipment description section, the resulting comparator design also enjoys very low drift (about 10 μvolts/^{o}C, -20^{o}C to +85^{o}C), high input impedance (10 megohms) and extreme simplicity.

3.0 ERROR ANALYSIS

The amount of precision required from a 10-bit ADC demands a close analysis of errors resulting from both its static and dynamic behavior. This section is devoted to a description of errors most commonly encountered in successive-approximation ADC's and suggests means for reducing or eliminating such errors. Also, error terminologies evolving from this and previous work are introduced and explained.

3.1 Types of Errors

Errors fall into two broad catagories--static and dynamic. Static errors are conveniently defined as those which are essentially independent of encoding speed. Examples are offset and gain drifts, non-linearities, and comparator hysteresis. Dynamic errors are those heavily dependent on encoding speed, such as are due to comparator response, ladder network ringing, and reference supply transient-load response. Amplifier random noise is also regarded as a dynamic error.

It is necessary to think of ADC errors in terms of their sources, in order to diagnose a design deficiency or trouble-shoot a manufactured unit, in spite of the difficulty of interpreting the erroneous digital code in terms of its analog source. One convention that should be followed is that the output code be made the independent variable. This is done by adjusting the analog input voltage until the exact center of the switching region between two adjacent code conditions occurs, and recording the corresponding analog input, which is then dependent. An example of this is shown in Figure 1a as a serial PCM data train (serialized ADC output) whose probability of occupying code condition 1100110001 is equal to that of occupying code condition 1100110000 at any instant.

This procedure eliminates the $\pm \frac{1}{2}$ bit ambiguity due to the quantizing effect which would exist if the output code were taken as the dependent variable. That is, unless ADC errors are large compared to quantizing error, allowing the output code to be a dependent variable makes it impossible to completely distinguish analog errors from quantizing error. The convention

is quite reasonable in light of the fact that the ADC is now the measured rather than the measuring instrument. It assumes only that all noise, which modulates the output code between two conditions, is strictly random, so that its effect is independent of the particular code condition, and this is a very workable assumption in practice.

Now, if the next lower switching point is obtained (Figure 1b) and its corresponding analog input voltage also recorded, the difference voltage between a and b is an accurate indication of the ADC's dynamic behavior at this point in its range. For example, the ADC-4 may be adjusted at zero and full scale so that each code increment equals exactly 5.0 millivolts for a 5 volt input range. If the difference voltage measured above is 5.5 mv, say, a dynamic error of 0.5 mv exists between these switching points. A term describing this condition has been coined:"non-symmetry". This term is used because the largest errors of this type usually occur at switching points adjacent to the more significant bits of the ADC and the switching point on the opposite side of the more significant bit (Figure 1c) is typically, say, 4.5 mv from it. In other words, the more significant bit is not symmetrically located between adjacent switching points above and below it. Data taken at several code conditions involving some of the same bits frequently reveals a non-symmetry pattern which can infer inadequate comparator response, short settling time for a particular bit, or the presence of synchronous noise affecting only particular codes. This is, therefore, a useful concept for diagnostic work.

A worst-case non-symmetry condition is one so extreme that a code condition is completely omitted. This is referred to as a "non-progression", and this term evolved from thinking of an encoder as a device producing a binary-counting progression when a ramp voltage is applied. Figure 1d is another way of illustrating these conditions. The left-most trace represents a slowly-increasing ramp voltage applied as an analog input to the ADC. The first waveform to the right is the uniformly-spaced staircase which would result from an ADC having good switching symmetry. The second waveform indicates a non-symmetry condition. The right-most staircase waveform illustrates a binary non-progression.

3.2 Error Diagnosis

Non-symmetrical or non-progressive code conditions may result from a variety of ADC errors, such as incorrect ladder network weighting, abnormal d-a switch transistor offset voltage or saturation resistance, inadequate settling time, inadequate reference supply transient-load response, poor comparator response, ladder network ringing, or synchronous noise on the analog input. Once non-symmetry or non-progression is recognized as a symptom, the error source can be isolated. Static errors such as ladder or switch transistor weighting will remain unchanged if the ADC clock rate is reduced. These errors can then be isolated using dc measuring techniques. The other error types mentioned are dynamic in nature and can therefore be exaggerated by increasing the clock rate. Waveforms within the comparator amplifier (within its dynamic range) frequently reveal settling time or response problems as badly-rounded pulse edges. Poor reference supply recovery, ladder ringing, or synchronous noise show up as "spiking" or "overshoot" in comparator waveforms. Finally, these error sources can be pinpointed by noting whether the degraded comparator waveform coincides in time or waveshape with waveforms at the analog input, reference supply, or ladder network. The practice of using the output code as the independent variable is also useful for obtaining temperature drift data, since it removes the effects of noise and quantizing. In the case of the ADC-4, temperature drifts are confined entirely to the comparator, reference supply, and d-a converter. Comparator offset drift constitutes most of the ADC drift at zero scale. It is interesting that comparator gain drift is also reflected entirely as an ADC offset shift. This can be understood by realizing that since the ADC's servo-loop operation results in a final null condition at the comparator input regardless of input voltage, changing its gain affects all points over its input range equally (by raising or lowering the decision-threshold voltage at its output), and such an effect is strictly an operating point or offset shift.

ADC gain drifts are due entirely to reference supply drift or d-a converter drifts. ADC-4 ladder network resistors cause negligible full-scale drifts. The transistor switches used in the d-a converter also contribute very small zero and full-scale drifts, but the full-scale drift is not entirely negligible

and is compensated as described in section 4.0. The reference supply may be monitored by a precision dc voltmeter to isolate its contribution to ADC gain drift. The unexplained gain drift (due to d-a switch transistors) and ADC offset drift (due to the comparator) can then be inferred even though the ac waveform generated within the d-a converter-comparator loop cannot be precisely measured except by another, higher-speed ADC.

3.3 System Noise Measurement

One additional means of describing errors has proven useful. Even though as mentioned before, the output code can be adjusted to eliminate the effects of random noise, a very accurate measurement of peak noise can be obtained directly from the output code. This technique involves choosing any switching point and recording the analog input voltage required to place the output code at the lower edge, say, of the region over which switching is obtained. The "lower edge" is where only rare "flashing", due to noise peaks, returns the output code to the higher code of the two. The analog input is similarly recorded for the upper edge of the region. The difference voltage is then an accurate measurement of the expanse of the region over which switching occurs, and this is aptly referred to as the "uncertainty band" of the ADC. It is a very good measure of the peak equivalent input noise since it includes noise of any origin.

The region between two switching points for which only one code condition obtains, is called the "certainty band". Obviously, a good design should have a much larger certainty band than uncertainty band for all code conditions, and this is the case for the ADC-4.

4.0 EQUIPMENT DESCRIPTION

Figure 2 depicts a typical airborne PCM system employing the asynchronous ADC. The PAM multiplexer furnishes time division analog data to the ADC. The programmer applies a start command for each serial data word to be encoded, and the digital multiplexer and serializer interlaces ADC words with digital words from other sources, then generates a serial PCM data train. It should be noted that only a single pulse (encode start) is required to synchronize the ADC with the remaining equipment.

4.1 Logic Operation

The ADC-4 is shown in block diagram in Figure 3. Figure 4 is a timing diagram for the unit. The operation of the ADC is as follows. The encoding cycle is initiated by the encode-start pulse, which sets the control flip-flop enabling the ADC clock oscillator. At the same time, a common reset pulse resets all register switches (switch transistors and storage register) to an all-ZERO's condition. (The sequencer counters have previously been reset, at the termination of the previous encoding cycle.) The first clock pulse advances the counters to a detected state which produces an output on the 2^9 matrix output line. A matrix blanking pulse is employed to remove unwanted "slivers" at the matrix outputs due to counter propagation delay. The 2^9 matrix pulse so generated is steered through the set-reset logic and sets the most-significant register switch. This results in a d-a converter output voltage of exactly 2.5000 volts at the comparator input divider. If the analog input voltage exceeds 2.5000 volts by as much as .00025 volts, the comparator output disables the AND gate which applies an individual reset command to the set-reset logic, and the 2^9 bit is retained.

However, if the input is slightly less than 2.5000 volts, the AND gate is enabled and the reset aperture pulse, which limits the decision time to 0.25 μsec and places the decision at the end of the bit to allow maximum settling time, is applied to a reset shaper internal to the set-reset logic. The reset shaper then generates a pulse which resets the 2^9 register switch. (Intermediate reset aperture pulses are ignored because the reset shaper is disabled until the 2^8 matrix output appears.) This is the bit-by-bit decision mechanism required for successively approximating the analog input. The process continues, with each retained bit adding its contribution to the d-a converter output,

until the 2^0 bit has been decided. At the instant a decision is reached on the 2^0 bit, the encoding cycle is stopped by the 2^0 reset pulse which also resets the control flip-flop and sequencer counters in preparation for the next encode-start pulse. Of course, the completed binary output is available at the time of the 2^0 decision and until the following encode cycle begins.

The set-reset logic scheme employed is one which allows close to the maximum possible settling time for each bit and is an important feature because bit settling time is a premium quantity here. A disadvantage of this scheme, when improperly implemented, is the possibility of a given decision being influenced by an incorrect comparator output due to the presence of the following bit, which is used to enable the reset shaper for the bit being considered. In other words, if the reset aperture pulse sufficiently overlaps the leading edge of a subsequent bit; the correct decision may be erroneously reversed due to the presence of the subsequent bit at the comparator output, which is applied to the reset shaper for the duration of the reset aperture time. This situation was circumvented entirely by designing register switch stages to have a set delay of about 0.5 μsec and a reset delay of less than 0.2 μsec (note the timing diagram). The result is that a "safety zone" of about 0.2 μsec exists between the reset aperture pulse trailing edge and the leading edge of the subsequent bit. This is consistent over the temperature range, so guarantees complete freedom from any interference between bits.

4.2 D-A Converter

The precision reference supply was designed to furnish +15 volts to the register switches. The choice of a reference voltage three times the full scale input amplitude of 5 volts was based on the following important considerations. Transistor switches considered and evaluated all had undesirably high saturation resistance (R_{SAT}) in the inverted connection at the emitter current needed for high-speed operation. For example, a chopper version (2N2185) of the 2N861 transistor selected as a PNP switch (Q1-Q10, Figure 14) has a typical inverted R_{SAT} of about 30 ohms at I_e = 2 ma, and I_b = 1 ma, while the unselected 2N861 has a typical R_{SAT} in the common-emitter connection of only 8 ohms at the same currents. Experimental data taken on four other transistor types (2N2432, 2N2004, 2N2005, 2N2006) shows an average increase of more than 50% in (inverted) R_{SAT} with a 65°C temperature increase. This would infer an R_{SAT} drift in an inverted PNP transistor of about 15 ohms. For the most

significant bit, whose ladder resistance is 4K ohms, this is an error of 0.37% or 0.12% referred to the input, which is intolerable. The forward-connected (common-emitter) transistor would change only about 4 ohms, however, which is a gain error of only 0.03% at the ADC input. Because of this, register switch transistors are driven in the normal common-emitter connection and the +15 volt reference and a 3:1 divider network at the comparator input effectively reduce the offset voltages by 3:1. Of course, these initial offsets are completely removed by the ADC offset adjustment and the only concern is that their temperature drift should be negligible. In practice, errors due to offset drifts of the register switch transistors used are on the order of .01% or less.

Use of a lower reference voltage and inverted-driven transistors has proven to be much more troublesome in practice. (Considerable hand-tailoring of ladder-network resistors on each manufactured unit has been required to compensate the large R_{SAT}'s encountered in at least one known instance.) And as explained, the problem of R_{SAT} change with temperature is more troublesome if the latter approach is taken.

4.3 Precision Reference Supply

The +15 volt reference supply employs two dual-chip (differential pair) transistors in a straightforward differential amplifier design. One input senses the precision internal reference voltage and the other samples the output voltage of the supply. The difference voltage is amplified in a second differential stage and applied as a correction signal to a series regulating transistor furnishing up to 100 ma of output current. The first amplifier stage includes a constant-current source to help maintain a correct operating point for the stage.

A problem common to all high-precision supplies is the precision internal reference voltage required. Standard cells cannot be used because of the severe environment. A precision temperature-compensated zener diode appeared to be the most attractive solution to the problem. An industry survey conducted by Dynatronics indicated that zener diodes with V_Z = 9.0 volts are most stable but those having adequate stability (about 0.01%, -20°C to +85°C) are available in only small quantities at a high price (about $100.00 each). The best readily-available type (Jedec 1N940) sells for about $40.00 and has a temperature stability of about 0.03%, which is marginal for this application. However, all of the several units of the 1N940 type observed by Dynatronics and others exhibit an "inverted-parabola" temperature drift characteristic as shown in Figure 6. Because this characteristic is

consistent, a thermistor compensation technique (Figure 15, R38-R41, VR2) was devised to reduce the zener's temperature drift. The R38, R39 combination provides compensation for increasing temperatures by increasing the zener current, which increases the zener voltage because of the zener's dynamic impedance. The R38, R39 network exhibits a much larger effect for increasing temperature than decreasing ones because the thermistor negative temperature coefficient causes a larger per cent change in the parallel combination going hot than going cold. This is because any combination (series or parallel) of fixed and variable resistors can produce a non-linear effect. The series combination of R40, R41 produces a similar effect for decreasing temperatures and has a small effect at high temperature.

As illustrated by Figure 6, the network can be adjusted (by selecting R38 and R40) to closely compensate a normal zener characteristic. Because of the consistency between zener diodes and the small drift being compensated, the compensation is non-critical and compensation tailoring to individual zeners is not usually required.

Another problem was that of supply response. Since the possible future use of digital gain calibration required that the supply output be varied by a step-function input at a rate of about 10 kc, a filter capacitance could not be used at the output. Two approaches to the problem were taken. First, the number of separate transistors in the feedback amplifier was kept to a minimum consistent with the gain needed, in order to minimize high-frequency phase shift. Second, capacitors C2 and C3 were used to provide high-frequency negative feedback, which prevents instability due to high-frequency phase shift. "Speed-up" capacitor C4 allows the amplifier to sense and correct for transient loads. These precautions were taken to allow use of the settling time calculations (Tables I and II) directly, neglecting the effect of supply transient-loading response. A recovery time of less than 3 μsec from a 60 ma load change and less than 0.5 μsec from a 3 ma load change has been achieved, which exceeds the requirement.

The supply features inherent short-circuit protection, and automatic reset on removal of short. The measured zero to full load (0 to 100 ma) regulation is better than 0.0003%. An overall temperature drift of only 0.5 mv referred to the analog input has been achieved, so the total contribution of the supply to ADC error is on the order of only 0.005%. It is felt that this design advances the art so far as accuracy under these environmental conditions is concerned.

4.4 Comparator

The comparator amplifier represented the most difficult design area because of the need for both wide bandwidth and high input impedance. The design employs two dual-chip transistors in a modified differential input configuration which offers greatly improved response and reduced input bias current as compared to the more conventional differential connection. One input senses the d-a divided output and the other accepts the analog input voltage directly. A constant-current source employed to improve common mode rejection achieves an equivalent input error for 0 to 5.5 volt common mode inputs of less than 0.4 mv (0.004%). A second dual-chip transistor provides a second stage of low-drift gain. Two cascaded emitter followers provide a single-ended output driver. All voltage gain is therefore confined to the two differential stages to minimize drift. Neither the differential stages nor the emitter followers can be driven into saturation, which is the desirable condition suggested earlier, and this feature provides constant comparator response essentially independent of input signal amplitude. Excellent agreement was obtained between the settling time calculations and the observed behavior of the unit developed.

The comparator design goal of f_{3db} = 300 kc has been achieved and the open-loop gain-bandwidth product approaches 400 mc. This extremely wide bandwidth (for an amplifier having an input impedance of greater than 10 megohms) was achieved partly by use of partially-bypassed emitter degeneration in the first stage (C7 and R12 of Figure 9). The amplifier draws an input bias current from the source of less than 0.5 μa, which corresponds to an input impedance of more than 10 megohms. An overvoltage protection circuit is included at the input, and -6 volts to +20 volts may be applied without damage or degradation of subsequent data. The d-a divider has a source impedance of about 1 k ohms which develops an error voltage of 0.5 mv (because of the 0.5 μa bias current). This gives rise to a very slight hysteresis effect because an <u>increasing</u> analog input voltage places an arbitrary switching point about 0.5 mv away from where it occurs when a <u>decreasing</u> analog input is applied. This hysteresis places a lower limit of 0.5 mv on the uncertainty band, but this is at least a two-fold improvement over units the author has observed before and amounts to only a 0.005% error. The equivalent input noise of the comparator is completely negligible. Finally, and most important, its measured drift errors are on the order of only 1.0 mv (0.01%) over the temperature range. This design is also considered to be an advance in the (comparator) amplifier art for the application.

4.5 Power Supply

The power consumption design goal of 8 watts required that all ADC circuits be given careful attention in order to minimize power required, consistent with speed. For example, all flip-flops used are welded-module devices needing only about 10 mw of power each, but these flip-flops operate reliably over temperature in the sequencer counter string with up to 750 kc input pulse rates. Other modular logic blocks are similarly efficient. Of course, as mentioned earlier, one reason for high-impedance operation of comparator and reference supply circuits was to reduce power consumption. Since adequate response and low power consumption are conflicting parameters, the tradeoff required especially careful attention for these two circuits. The requirement that a $\pm$ 4.2 volt dc variation with 3 volt peak-to-peak random noise be applied to the +28 volt input power without affecting ADC accuracy also contributed to power consumption since the power supply must accommodate these input excursions by allowing a voltage-drop safety factor across its regulating elements. Also, the ADC is fully isolated from input power by means of a bifilar and sector-wound toroidal transformer, and transformer losses increase the power consumption slightly. Although the dc-dc converter operates at a low power level (efficiency is typically poor for low power operation) and chops at a 5 kc rate (which usually causes prohibitive transformer losses) to achieve the miniaturization required, its overall efficiency is about 73%. The total ADC input power is about 7 watts.

The dc-dc converter employs high-voltage stud-mounting silicon switching transistors as choppers and has a total idling power of less than 1.5 watts. It includes a series high-current diode at the input to provide reverse-voltage protection. Bridge rectifiers are used to avoid center-tapped secondaries, The basic series regulator design, which is duplicated for all three voltages, uses a dual-chip transistor as a differential feedback amplifier and a zener reference diode excited by the supply output. Short-circuit protection with automatic reset on removal of short is provided by this circuit, and internal current limiting protects against overloads. Overall temperature stability is about 2% and zero to full-load regulation approximates 1%.

Stud mounting transistors are used because of the difficulty of reliably dissipating heat in a hard vacuum by any other means than conduction. Supply reliability is further enhanced by the transistor choice, 2N1769, which has a 40 watt rating and is therefore in very conservative service.

4.6 Packaging

The overall packaging concept was developed by NASA-MSFC for use on their large-scale space vehicles.

The ADC is contained on eight printed cards, four of which contain analog circuits (comparator, register switches, reference supply, and power supply). The remaining four cards are logic circuits containing a total of 15 welded modules, several of which contain more than one circuit (timing, sequencer, set-reset logic, and reset and blanking circuits). Analog cards are fully printed to permit adjustment and troubleshooting. Logic cards interconnect welded modules but also contain a few special-purpose, one-of-a-kind logic circuits (shapers, etc.) to satisfy drive or other requirements.

The external package for which the ADC has been developed is a magnesium casting employing the floated, compression-suspension principal to support the printed-circuit cards. This package is used for all types of instrumentation employed by NASA-MSFC in flight testing of recent large scale space vehicles. The package is very effective in "softening" the environment to which the ADC is subjected and contributes considerably to the ability of the unit to operate with full accuracy under the severe missile environment.

All circuitry is silicon solid-state employing the most recent, most reliable devices available during the course of the development effort. Welded modules used have been proven in two other space applications. Printed cards are gold-plated and, as far as is known, are subjected to the most stringent manufacturing and inspection requirements of the missile/space industry.

5.0 ZERO AND GAIN CALIBRATION RECOMMENDATION

5.1 General

The zero and gain calibration approach described below is an outgrowth of two previous schemes, combining the better features of each (acquisition indication, digital storage, command synchronization, and unlimited resolution) and eliminating the undesirable features (overrange cycling, "searching ripple", and quantizing doubling). It has the additional advantage of performing a check on the calibration circuitry by allowing the ADC itself, following calibration, to encode the calibration voltage for transmission.

The zero and gain calibration timing diagram is shown in Figure 7. A zero or gain calibration function takes place during the first half of a calibration interval, which is equal in length to an encoding interval. The remainder of the encoding interval is used to verify the calibration by allowing the ADC's six lesser significant bits to run through an encoding cycle. Since the correct calibration code is predetermined, the ADC's resulting output presents an immediate indication of calibration acquisition (or non-acquisition).

Correction ranges of both zero and gain calibration circuits are 128 mv. The corrections are available in two steps of 2 mv each during one correction interval. Limiting the number of correction steps to two per interval allows the calibration to be done in one-half a normal encode cycle and also allows the corrections to cancel (one plus, then one minus) if the original error was less than two millivolts. Calibration ripple, the "hunting" of the least significant correction, is eliminated in this manner.

During the first half of the calibration interval, the calibration circuitry is controlled by the gated ADC clock. The calibration to encoder loop is closed through the comparator, which makes the adjustment decisions in the same manner in which it ordinarily makes code decisions. Error is limited to plus or minus one-half the least significant correction step and the hysteresis error of the comparator ($\pm$ 1.5 mv total error due to calibration).

5.2 Logic Operation

The calibrate cycle is initiated during the word time just previous to the interval used for calibration. The calibrate command is then stored until the normal encode start command

starts the calibration cycle. The initiate logic performs the functions of synchronizing the calibrate interval with the normal encoder start command and of selecting either zero or gain calibration. Referring to the zero and gain calibration logic diagram, Figure 8, it can be seen that the initiate logic provides selection information to the advance-retard logic, calibration code set logic, and the forward-backward counters. The matrix blanking and step pulse generator receive a start command for calibration of either end point. Upon receiving a zero or gain calibrate signal and the encode start command, the initiate logic commands the matrix blanking, the calibration code set, and the counter selection portion of the advance-retard logic such that the following conditions exist: (1) the matrix output is disabled (the ADC sequencer counters are in normal operation); (2) the register switches are set to a predetermined condition (corresponding to the input analog calibration voltage); (3) the output of the advance-retard logic is gated to the corresponding F-B counter; and (4) the step pulse generator is enabled.

The step pulse generator contains a matrix to decode three states of the ADC counters. The first state is used as the trigger to step the F-B counters; the second decoded state provides the second F-B counter trigger, and the third state provides a stop command for the calibration circuitry.

The advance-retard logic, commanded by the output of the comparator, gates the first and second step pulse triggers to either advance or retard the forward-backward counters. The comparator output depends (as in normal operation) on whether the analog input is greater or smaller than the d-a output. For gain calibration, the +15v reference supply is adjusted by the gain F-B counter. For zero calibration, the d-a input at the comparator is modified by a resistively-summed input from the zero F-B counter.

The F-B counter string is twice stepped, by the step pulse triggers and the advance-retard logic, to increase or decrease the adjustment voltage up to 4 mv's in either direction in a single calibrate interval. The total correction range is ± 64 millivolts. The F-B counters have overrange limiting which forces the correction to stay at maximum without recycling if the calibration voltage exceeds the range in either direction.

The third decoded state of the counters is used to reset the six least significant register switches and to disable the calibration circuitry. The ADC may then encode the calibration voltage at the comparator input in a normal manner, except that only

the 2^5 through 2^0 bits need to be encoded (the 2^9 through 2^6 bits remain set in the correct code condition). Then the output code at the end of a calibration interval verifies the calibration of the unit to the applied input.

6.0 CONCLUSIONS AND RECOMMENDATIONS

6.1 Test Results

Now that the design guidelines and individual circuit descriptions have been discussed, it is appropriate to conclude this document with a recitation of the important performance characteristics of the finished unit. The reader is referred, for comparison, to the DESIGN APPROACH section which lists all design goals of the development program.

Both NASA-MSFC and Dynatronics employ automatic plotting devices which contain a precision d-a converter slaved to the ADC under test, a precision ramp generator, an error comparator, and a graphic recorder.

The difference between the d-a converter output (which appears as a staircase waveform as in Figure 1d) and the ramp generator (also shown in Figure 1d) is plotted vs time. The result is a sawtooth waveform accurately displaying the quantizing error and the ADC's static and dynamic behavior. Figure 5a is a plot of an ADC-2 having a non-symmetry condition not easily spotted on a "quick-look" type binary display. Figure 5b is a plot of the ADC-4.

Measured accuracy is 0.03% absolute, -20°C to +85°C, and includes errors from all sources at all 1,024 binary code conditions at the output.

The ADC has been operated at conversion rates exceeding 25 kc (word rate) over the temperature range, at full accuracy. The input impedance exceeds 10 megohms, including input bias current, and is virtually independent of the input voltage applied. A reliability figure of 12,000 hours mean-time-before-failure has been obtained following the commonly-accepted component-bit-failure rate approach, which assumes that a failure of any single component results in a system failure. Comprehensive environmental testing of the ADC has been successfully accomplished at NASA-MSFC.

It is gratifying that, as the reader will note, every design goal of the development effort has been met or exceeded.

6.2 Recommended Additional Development

The accuracy-speed-power trade-off was made somewhat in favor of accuracy here. A further accuracy improvement could hardly be justified, in view of present transducer accuracies. However, the technology developed and employed (variable-speed encoding,

wide bandwidth comparator) could be further developed to obtain a substantial speed increase at little sacrifice in accuracy. Such a speed improvement would probably require development of a low-drift single-ended input comparator amplifier having a low input impedance and operating at much lower internal impedance levels. Such a design appears necessary in order to obtain the required bandwidth and eliminate the hysteresis effect (which would worsen in inverse proportion to input impedance.) Of course, a buffer amplifier would then be needed to provide an adequately high input impedance.

Another possibility is that of reducing the ADC power requirement. Two approaches warrant consideration. First, dc-dc converter efficiency might be improved by use of a narrow-hysteresis-loop core material ("Supermalloy", for example) to reduce core losses. It may even be possible to eliminate the transformer, employing instead charge transfer techniques which can also achieve a high degree of isolation at higher efficiencies (perhaps 90%). Second, system power itself can be reduced by a careful evaluation of the R_{SAT} problem in register switches, with the aim of reducing their drive requirements while maintaining low R_{SAT} drift.

At the same time speed and power improvements are sought, a substantial reliability gain and a reduction in size and cost could be achieved by use of fully-integrated logic. For example, integrated flip-flops (full binary, J-K type) are now available in TO-5 cans at about one-half the cost of series 300 welded flip-flops. (Such integrated logic is used in a current aerospace development effort conducted by the writers.) Most circuitry now on the timing and control, sequencer, set-reset logic, and reset and blanking cards could be replaced with integrated logic elements. However, it is not anticipated that linear integrated circuitry will become available in the near future which can achieve the performance required of the discrete-component circuitry developed for the comparator, register switches, +15 v precision reference supply, or power supply cards. These circuits could be packaged in welded module form, though. With the integrated logic also packaged in welded modules, it is estimated that a reduction in ADC volume of better than 2:1 could be achieved. In other words, the entire basic ADC could be contained on four (possibly three) 4.3" x 3.2" cards. Gain and zero calibration logic described in section 5 should also be implemented using integrated logic, and could probably be contained on one additional card.

All of the foregoing paragraphs, then, serve as a recommendation for ultimate, long-range improvements in circuitry and packaging using the ADC-4 as a starting base.

The following paragraphs suggest certain immediately-realizable improvements which do not require circuit configuration changes. (These are aside from minor refinements which may result from ADC-4 production and cannot be anticipated.)

First, it is recommended that the Model 301 motherboard be modified to isolate primary and secondary power grounds. Then removal of the ground strap on the ADC-4's power supply allows it to provide isolation. The isolating supply for the PCM package could then be deleted, which would result in an overall power savings. Another possibility is that of further reducing ADC-4 drift by special specification of critical dual-chip transistors (Q1, Q2, Q3, Comparator; Q3, Q4, +15 v Precision Reference Supply). It should be possible to obtain lower-drift, selected versions of these transistors at somewhat greater cost.

A significant improvement in ADC-4 reliability could be obtained by substitution of metal film resistors for all wirewound units (Comparator, +15 v Reference, and Ladder Network). (A bit-failure rate calculation shows a reliability increase of nearly 5,000 hours MTBF when metal film resistors are used.) A metal-film ladder network has been used in the ADC-4 prototype and is completely satisfactory. The low temperature coefficients required make the network quite expensive (about $300.00), compared to a wirewound network (about $80.00), which is the reason wirewound resistors were chosen.

Finally, and most significant, the entire ADC-4 could be re-packaged in cordwood welded modules. Nearly all components used in the present design have or are available with weldable leads. All resistors, diodes and (almost all) capacitors are the same physical size, that of a one-quarter watt resistor, since they were chosen with the idea of welded packaging in mind. These components require a module height of about one-half inch, when mounted vertically, so card spacing would have to be increased somewhat. Extremely dense packaging (more than 120 normalized components per cubic inch) has been achieved in Dynatronics standard airborne modules. It appears very likely that a reduction in ADC volume of nearly 2:1 could be achieved by this means, so that the basic ADC could be contained on four (or five) 4.3" x 3.2" cards. Possibly two additional cards would be required for gain and zero calibration circuits. Of course, an inherent disadvantage is circuit inaccessibility. Since ADC-4 drift is confined to a very few components which

From: $E=E_f\,\varepsilon^{-\frac{t}{RC}}$, $\frac{E}{E_f}=\varepsilon^{-\frac{t}{RC}}$; Then: $\frac{E}{E_f}$ x 100% = % short of E final

TABLE Ia

t	$\frac{E}{E_f}$ x 100%
2 μsec	13.600 %
4 μsec	1.850 %
6 μsec	.300 %
8 μsec	.034 %

TABLE Ib

(3 db point at 160 kc, RC = 1 μsec)

Bit	Contribution at Input (%)	Arbitrary Settling Times (μsec)	Error Referred to Input (%)
2^9	50.0000	8	.0170
2^8	25.0000	8	.0085
2^7	12.5000	6	.0370
2^6	6.2500	6	.0190
2^5	3.1250	4	.0575*
2^4	1.5650	4	.0290
2^3	.7810	4	.0150
2^2	.3900	2	.0050
2^1	.1950	2	.0025
2^0	.0975	2	.0012
		46 μsec total	(*high)

TABLE IIa

(Using RC = .53 μsec)

t	$\frac{E}{E_f}$ x 100%
2 μsec	2.300 %
4 μsec	.054 %
6 μsec	.010 %

TABLE IIb

(3 db point at 300 kc, RC = .53 μsec)

Bit	Contribution at Input (%)	Arbitrary Settling Times, ≤.01% Error	Error Referred to Input (%)
2^9	50.0000	6	.0050
2^8	25.0000	6	.0025
2^7	12.5000	4	.0070
2^6	6.2500	4	.0035
2^5	3.1250	4	.0017
2^4	1.5650	4	.0008
2^3	.7810	4	.0004
2^2	.3900	2	.0090
2^1	.1950	2	.0045
2^0	.0975	2	.0022
		38 μsec total	

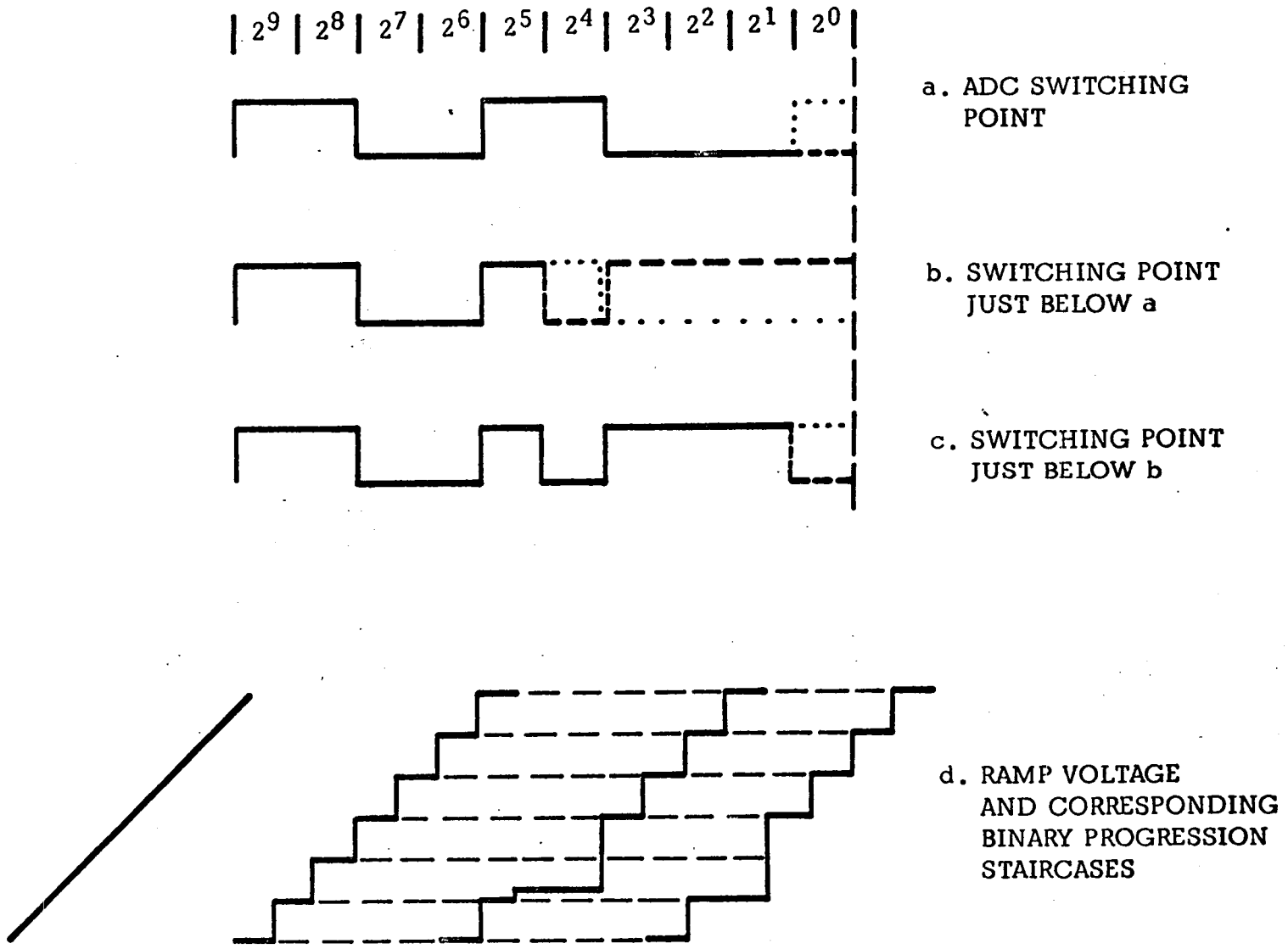


FIGURE 1

#7192

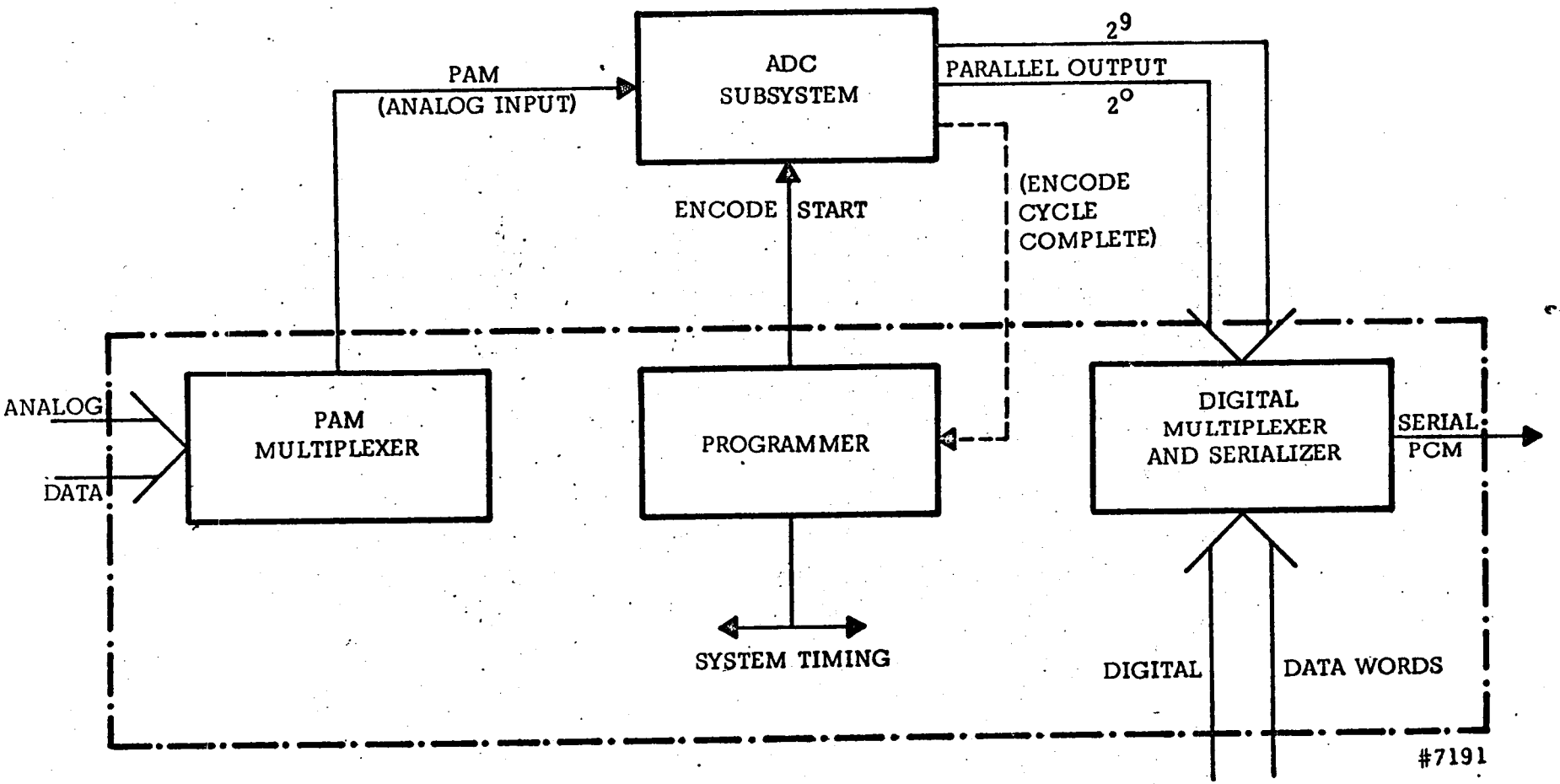


FIGURE 2. AIRBORNE PCM SYSTEM

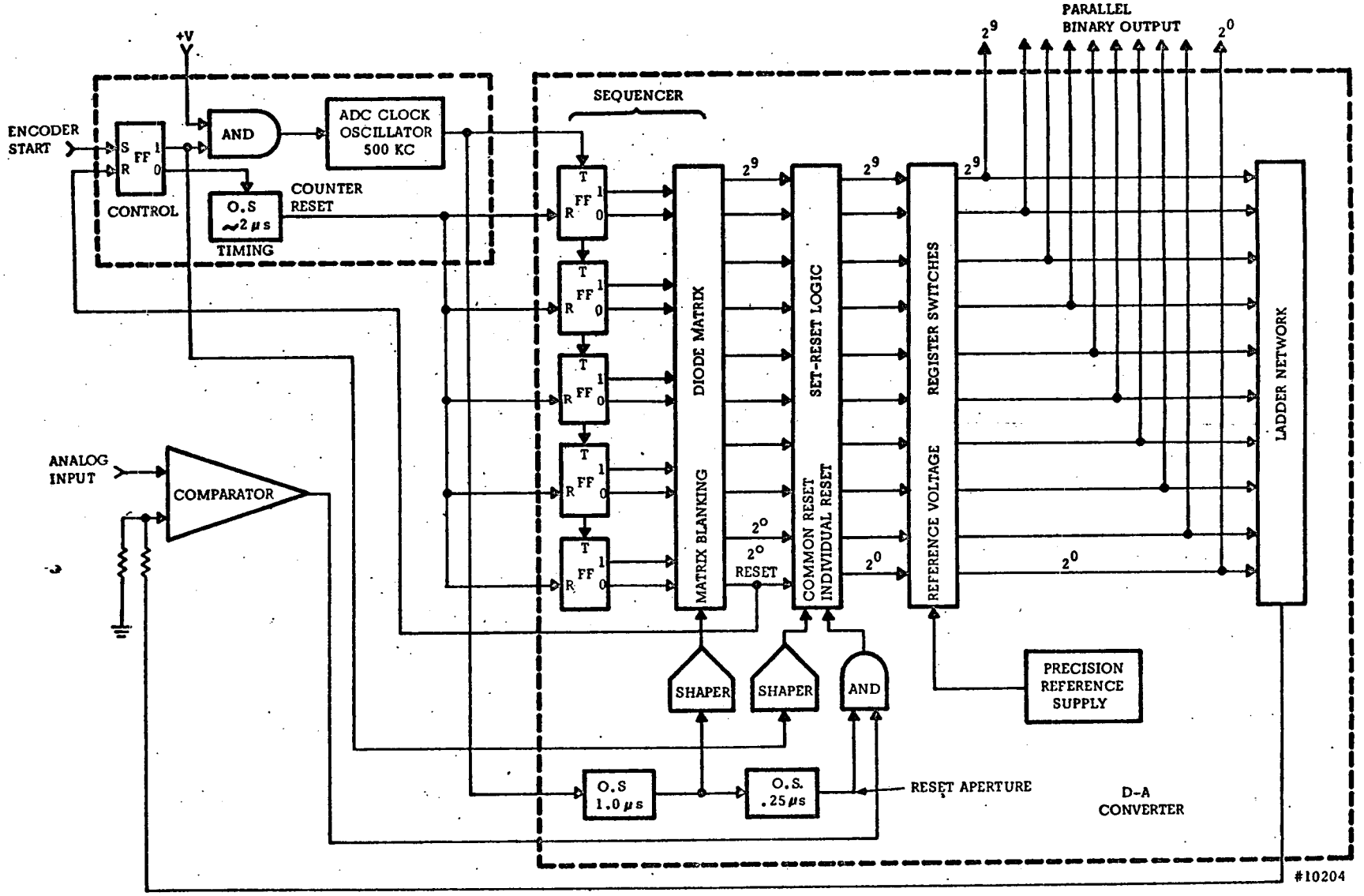


FIGURE 3. ADC LOGIC DIAGRAM

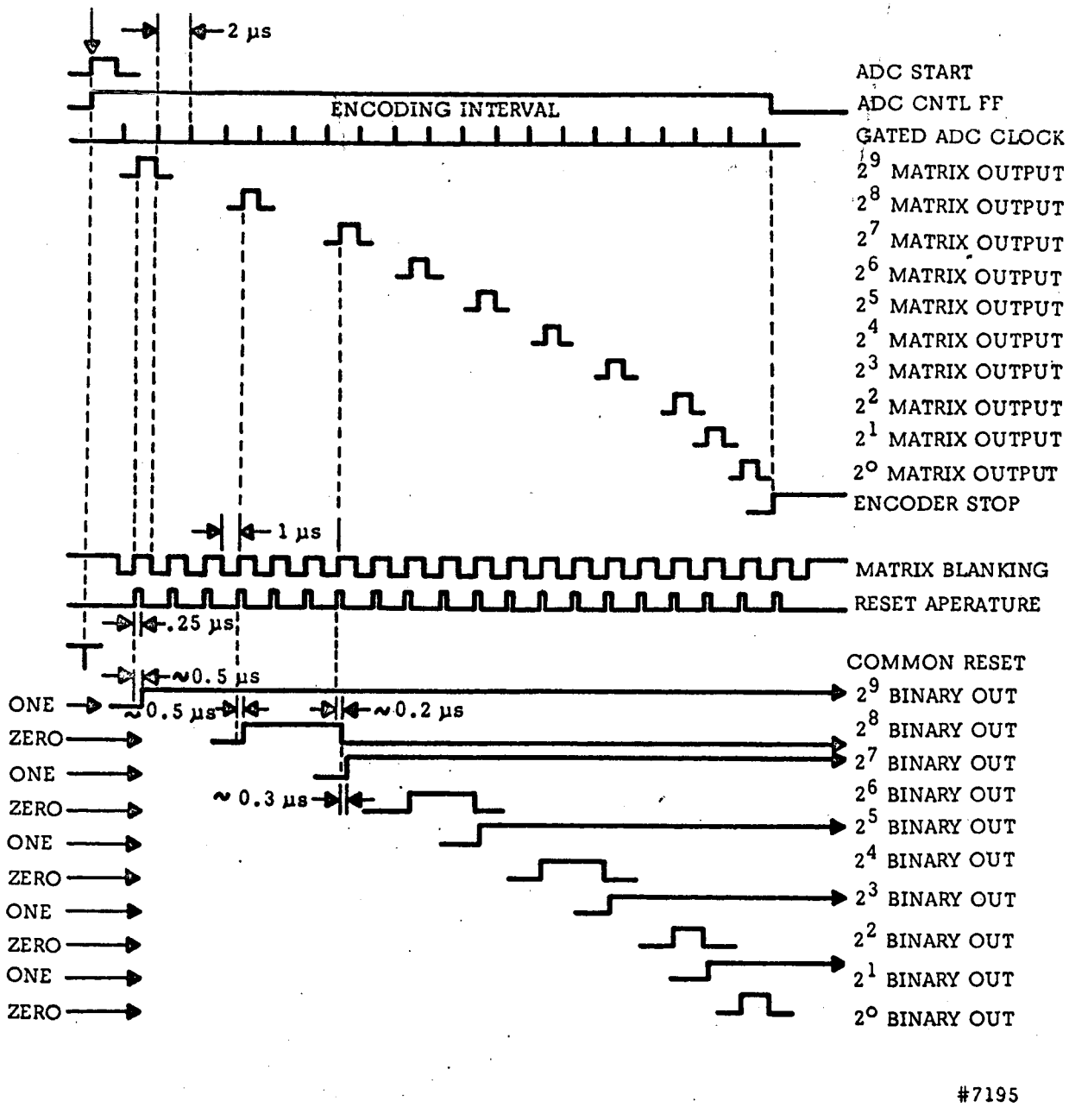


FIGURE 4. ADC TIMING DIAGRAM

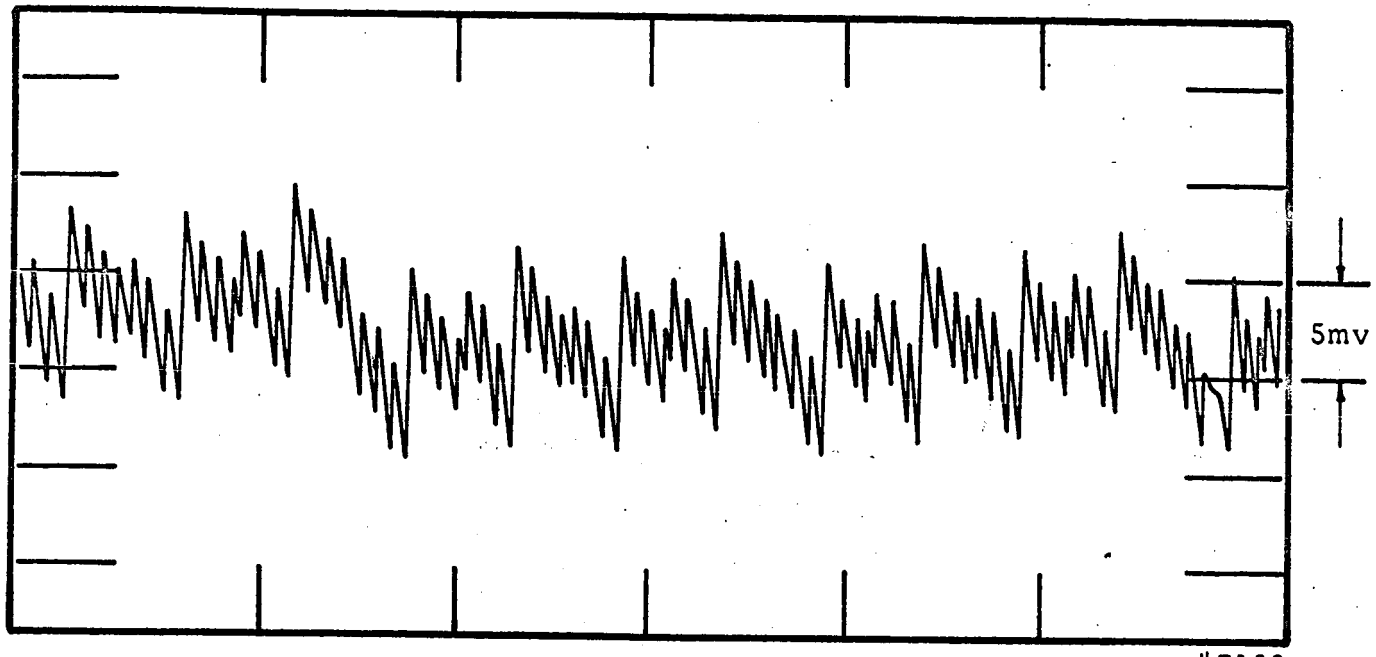


Figure 5a

#7193

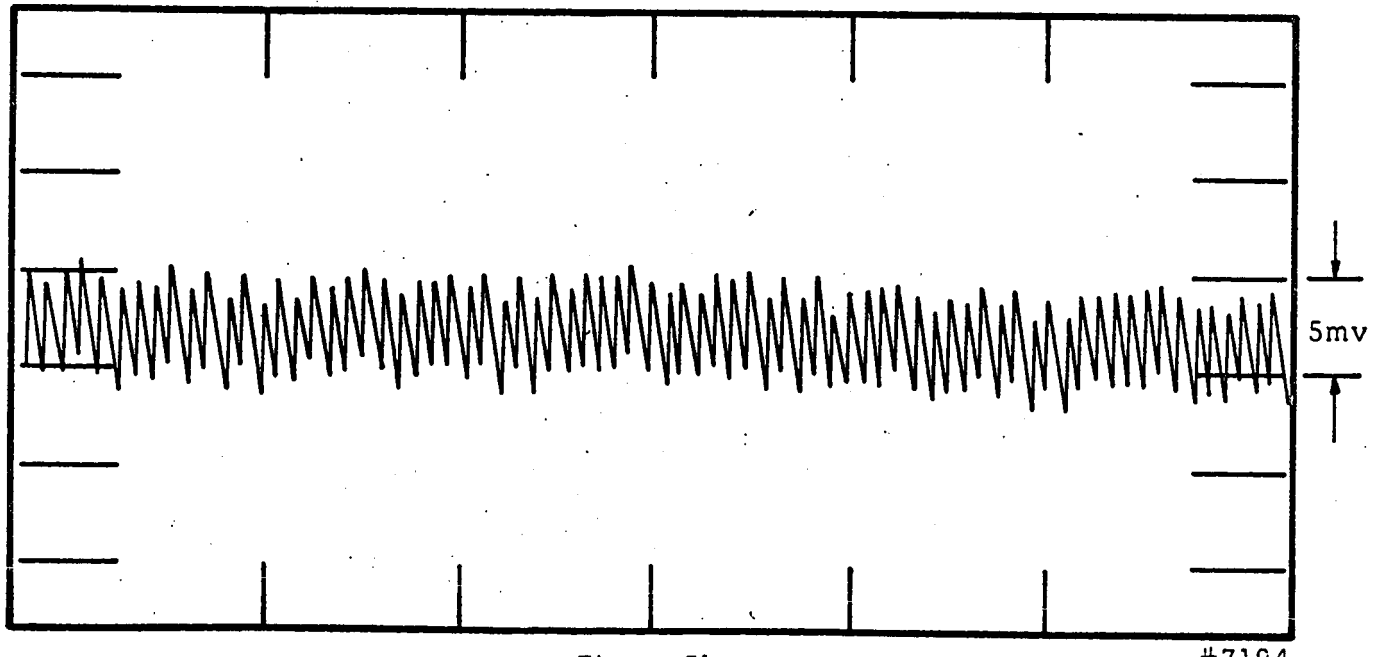


Figure 5b

#7194

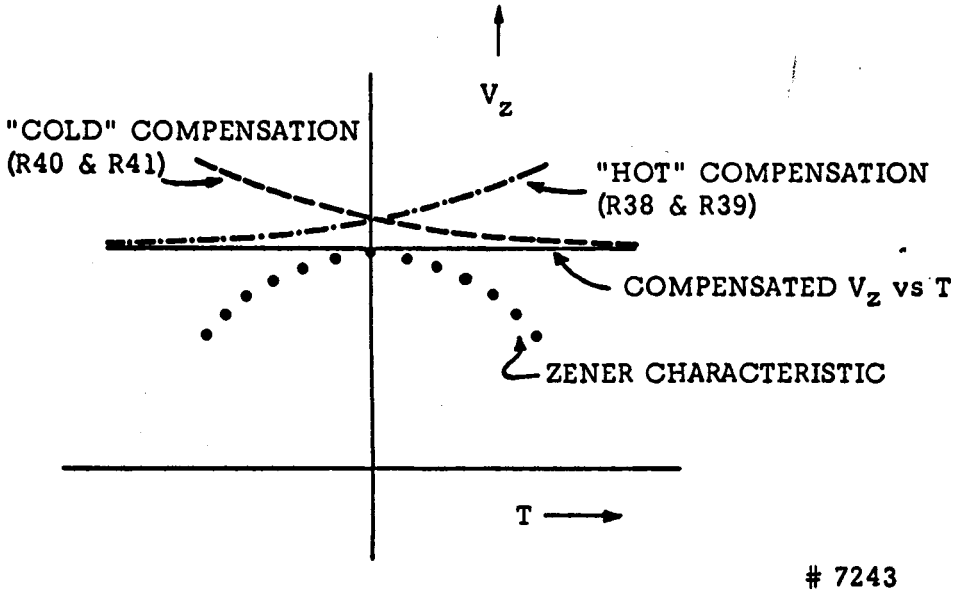


FIGURE 6.

PRECISION ZENER REFERENCE DIODE COMPENSATION

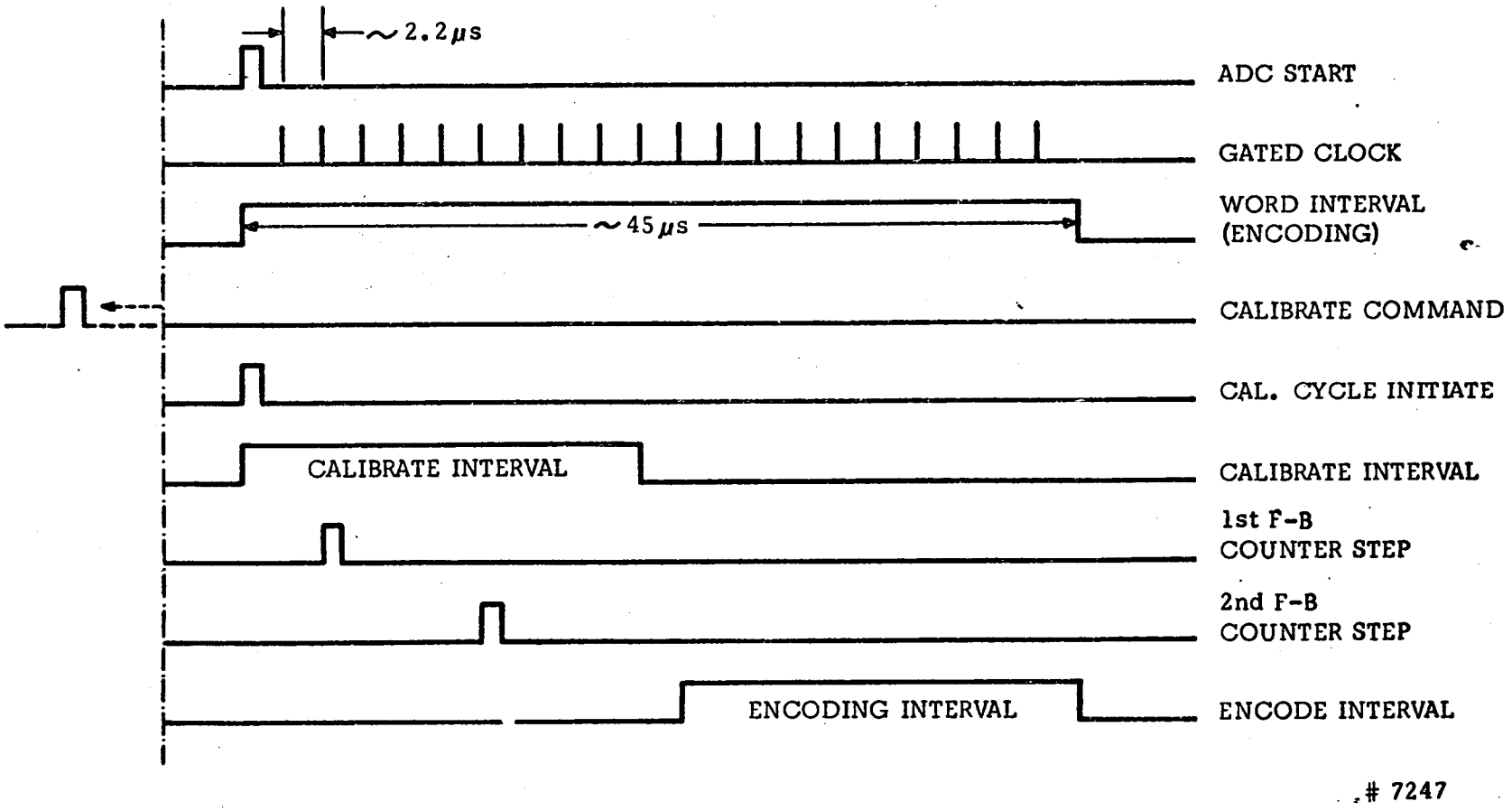


FIGURE 7. ZERO AND GAIN CALIBRATION TIMING

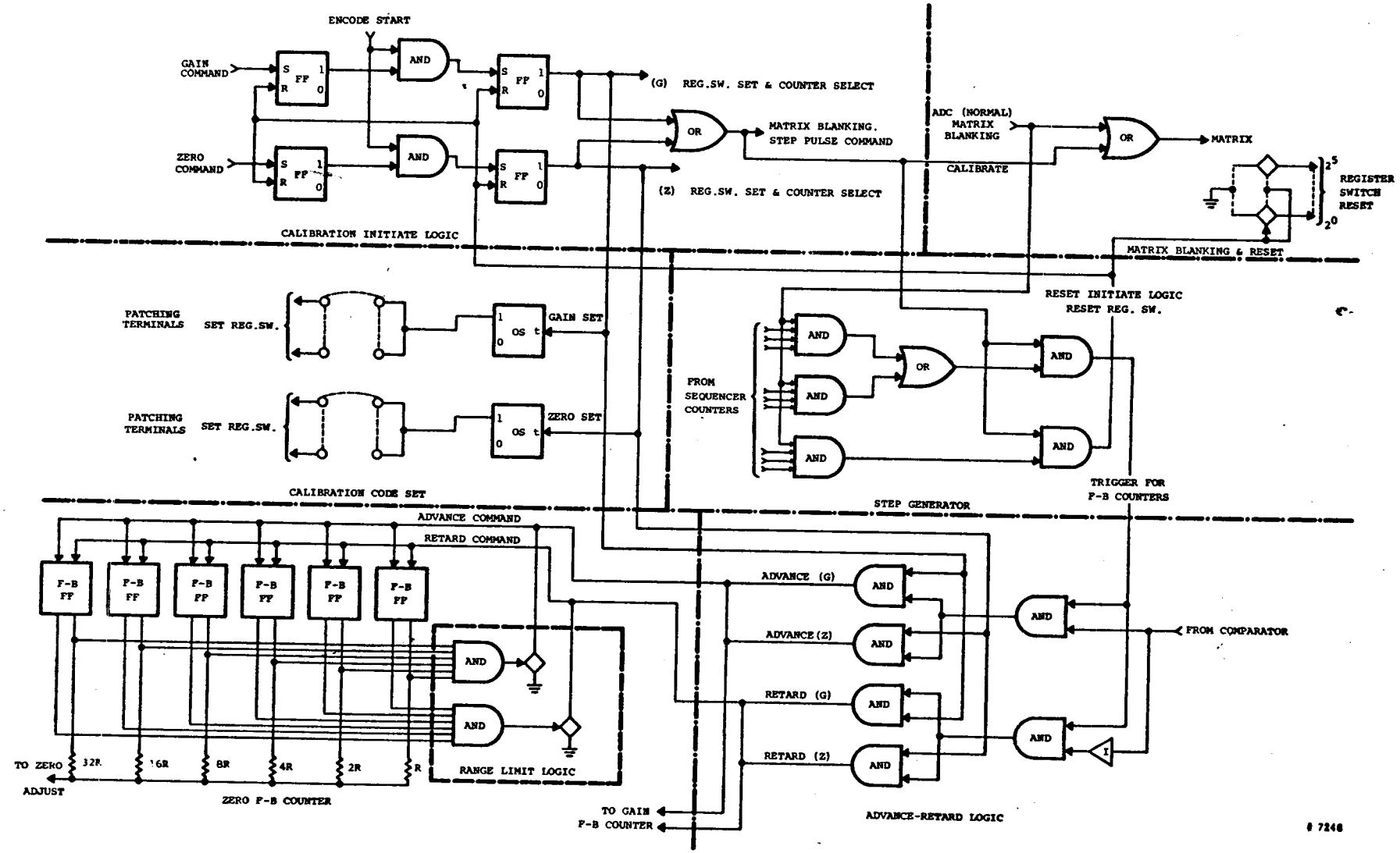
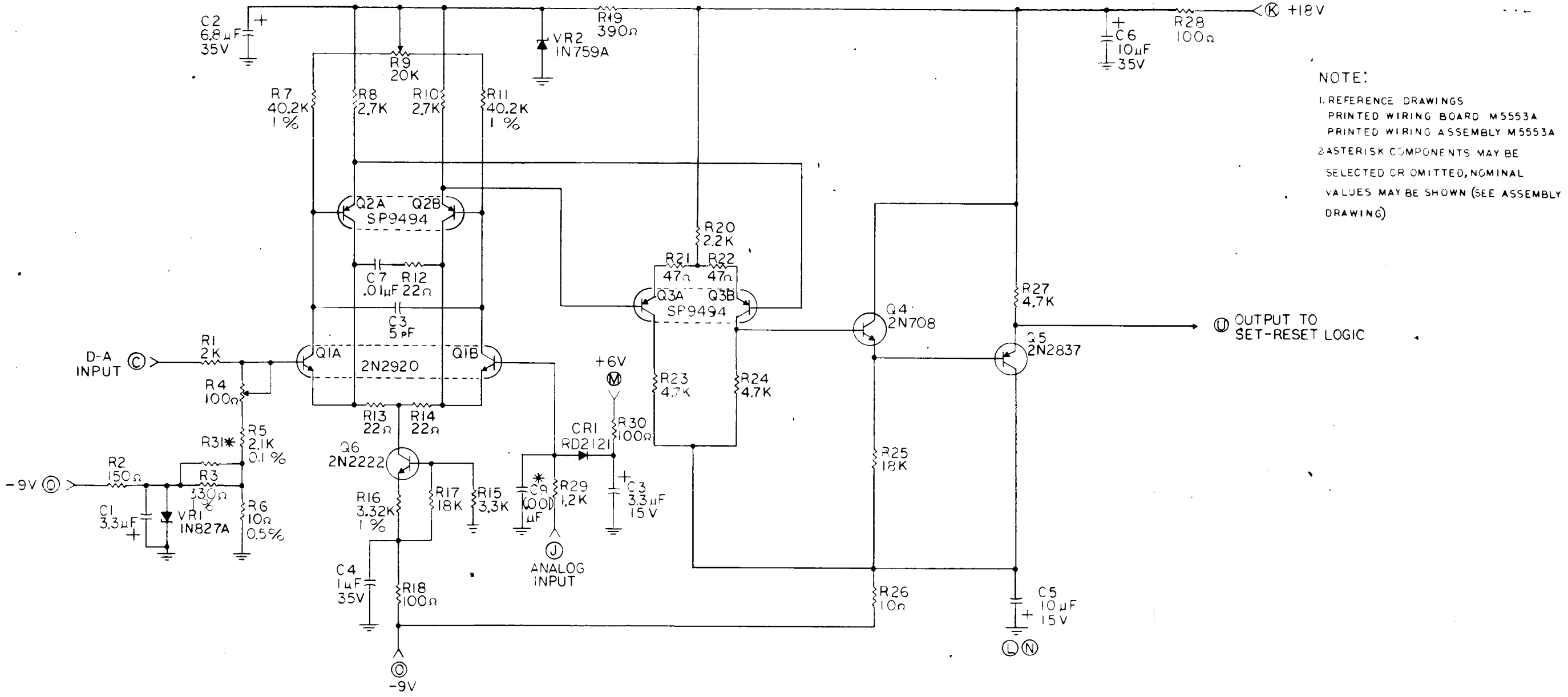


FIGURE 8. ZERO AND GAIN CALIBRATION LOGIC

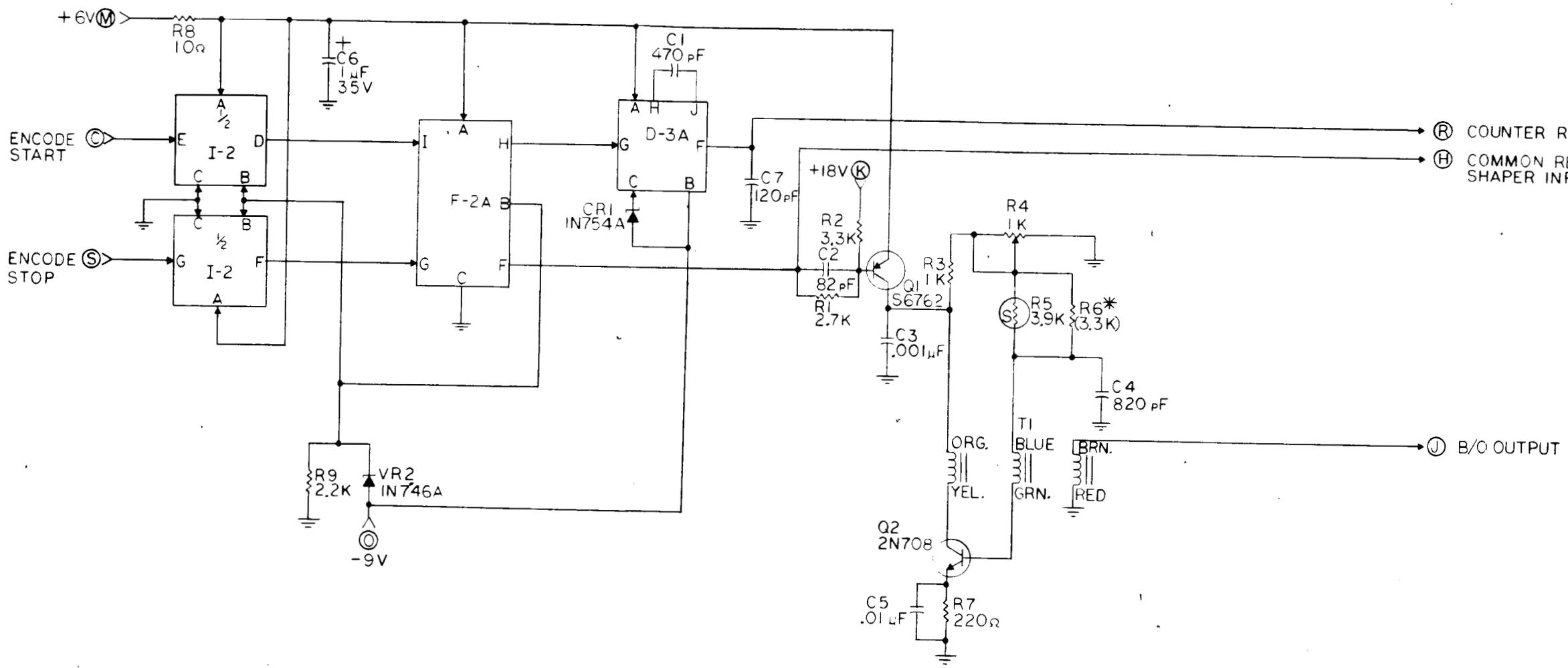


NOTE:

1. REFERENCE DRAWINGS
   PRINTED WIRING BOARD M5553A
   PRINTED WIRING ASSEMBLY M5553A
2. ASTERISK COMPONENTS MAY BE SELECTED OR OMITTED, NOMINAL VALUES MAY BE SHOWN (SEE ASSEMBLY DRAWING)

[illegible]
[illegible]

FIGURE



NOTE:

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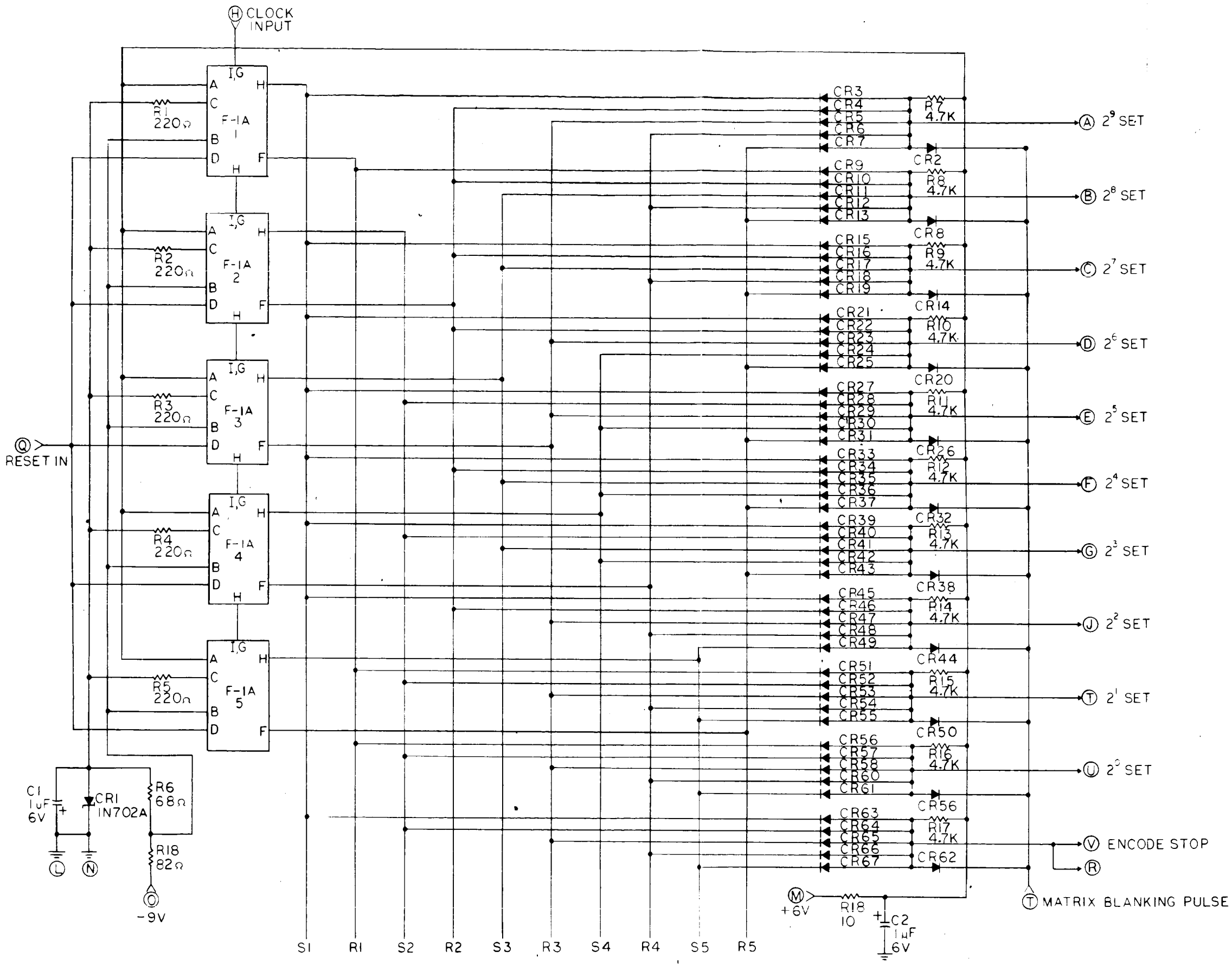
   PRINTED WIRING ASSEMBLY M5554A
2. ASTERISK COMPONENTS MAY BE SELECTED OR OMITTED, NOMINAL VALUES MAY BE SHOWN. (SEE ASSEMBLY DRAWING)

TIMING & CONTROL SCHEMATIC
PC [illegible]-M5554A



NOTES:

1. REFERENCE DRAWINGS
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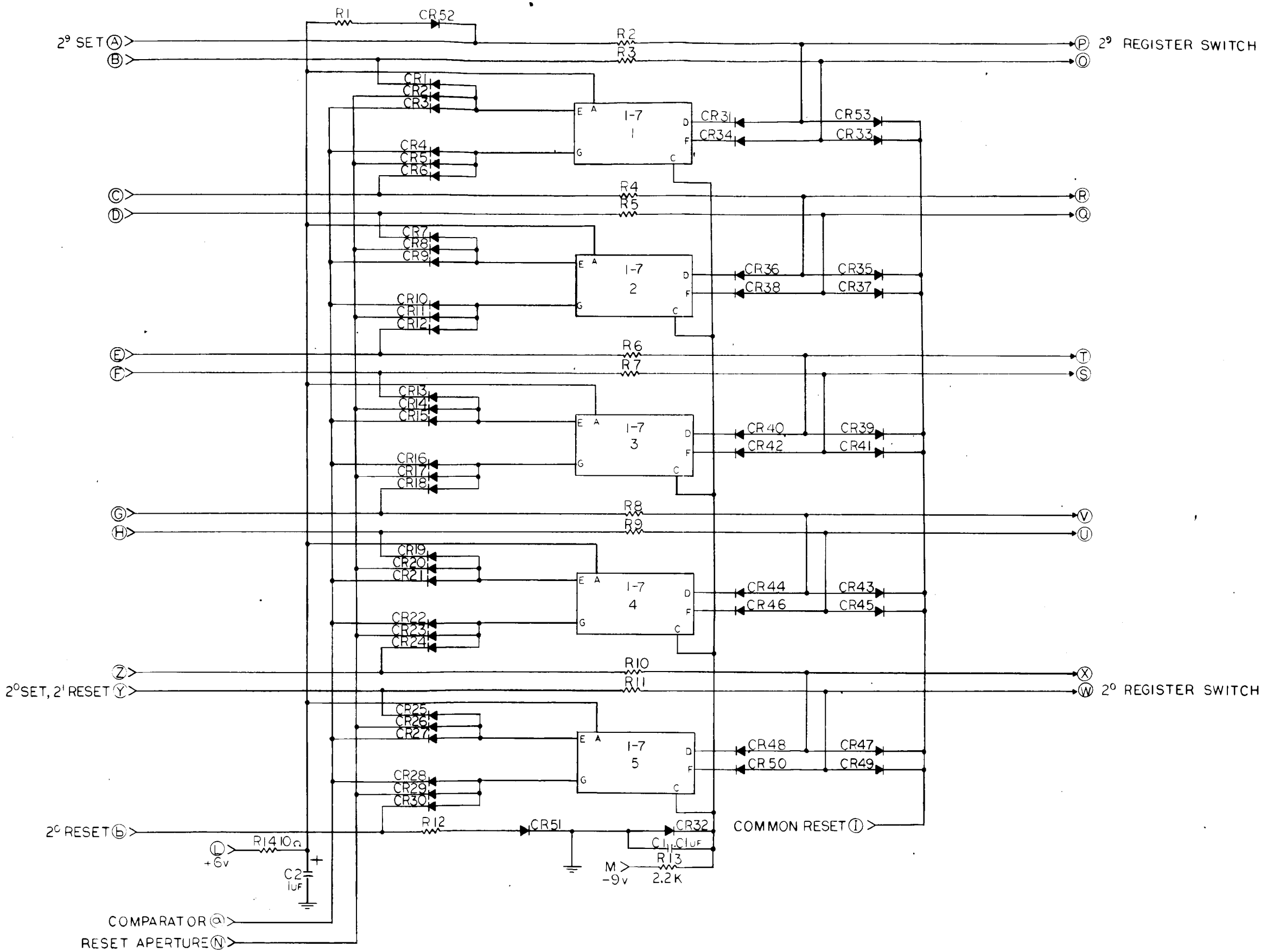
2. UNLESS OTHERWISE SPECIFIED:
   DIODES – RD2121



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
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   RESISTORS ARE 4.7K, 1/4W, 5%
2. REFERENCE DRAWINGS M5556A
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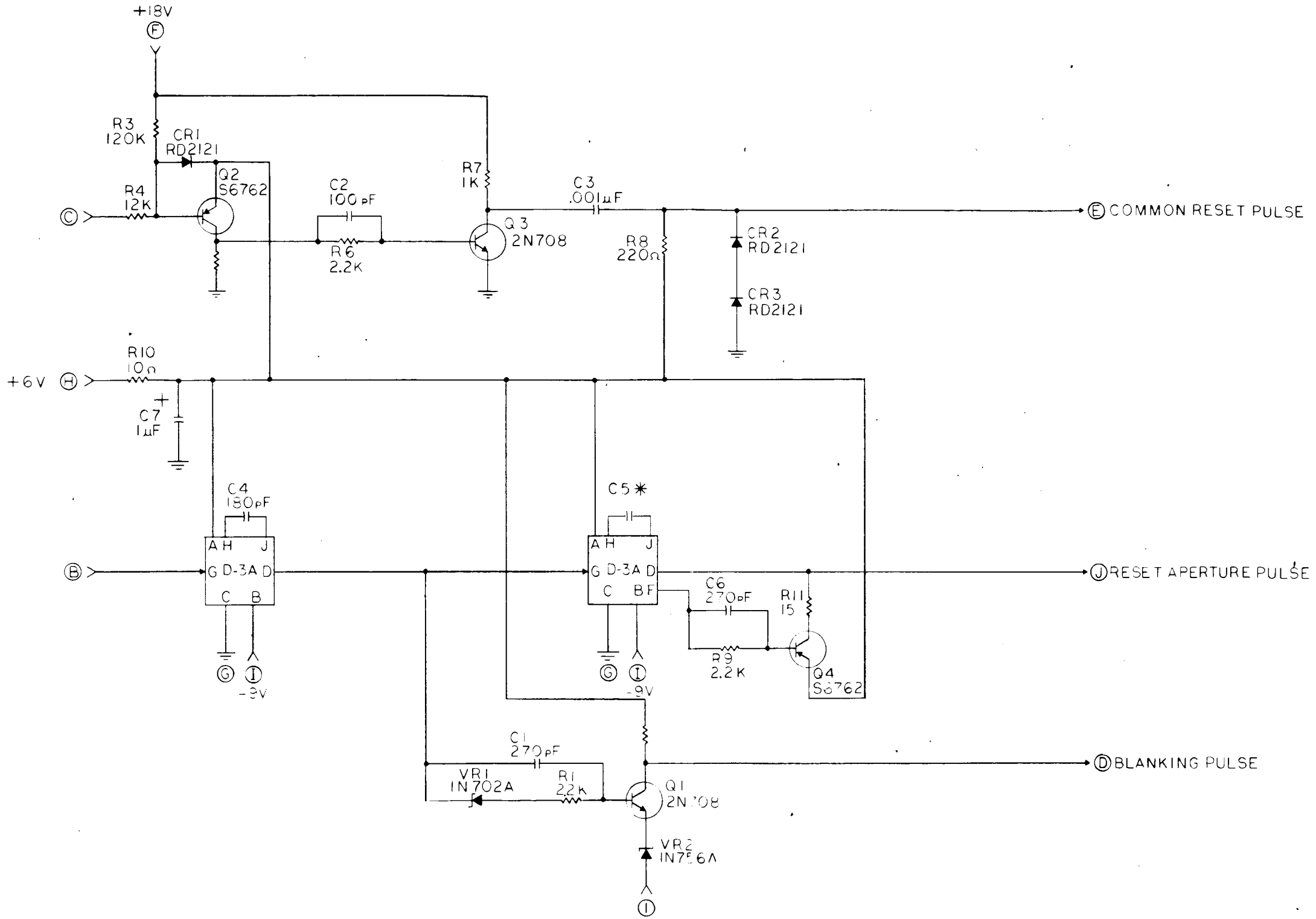
   PRINTED WIRING ASSEMBLY
   M5556A



NOTE:

1. REFERENCE DRAWINGS
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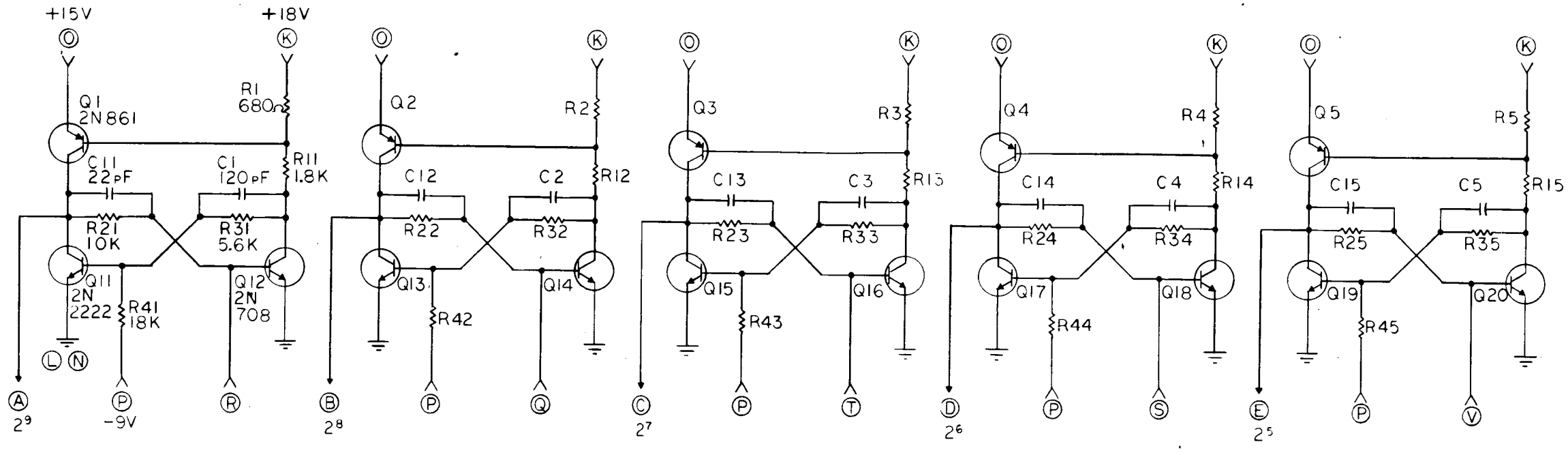
   PRINTED WIRING ASSEMBLY M5557A
2. ASTERISK COMPONENTS MAY BE SELECTED OR OMITTED, NOMINAL VALUES MAY BE SHOWN. (SEE ASSEMBLY DRAWING)

BLANKING



NOTES:

1. REFERENCE DRAWINGS
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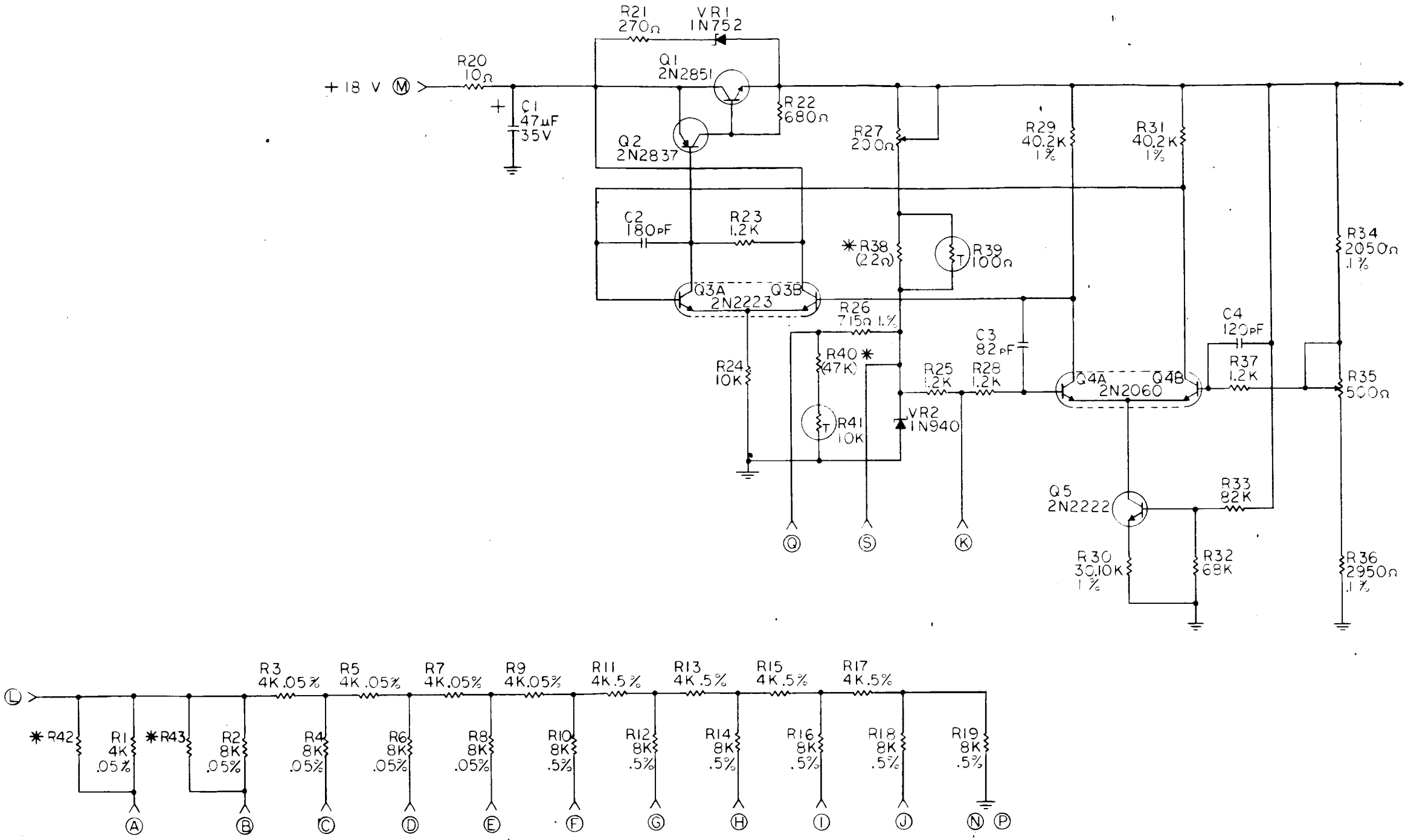
   PRINTED WIRING ASSEMBLY M5558A
2. UNLESS OTHERWISE SPECIFIED:

Q1 – Q10	2N861, SELECTED PER. D. I. SPEC.
Q11,Q13,Q15,Q17,Q19,Q21,Q23,Q25,Q27,Q29	2N2222
Q12,Q14,Q16,Q18,Q20,Q22,Q24,Q26,Q28,Q30	2N708
R1 – R10	680Ω ¼W 5%
R11 – R20	1.8K
R21 – R30	10K
R31 – R40	5.6K
R41 – R50	18K
C1 – C10	120pF
C11 – C20	22pF



NOTE:

1. REFERENCE DRAWINGS
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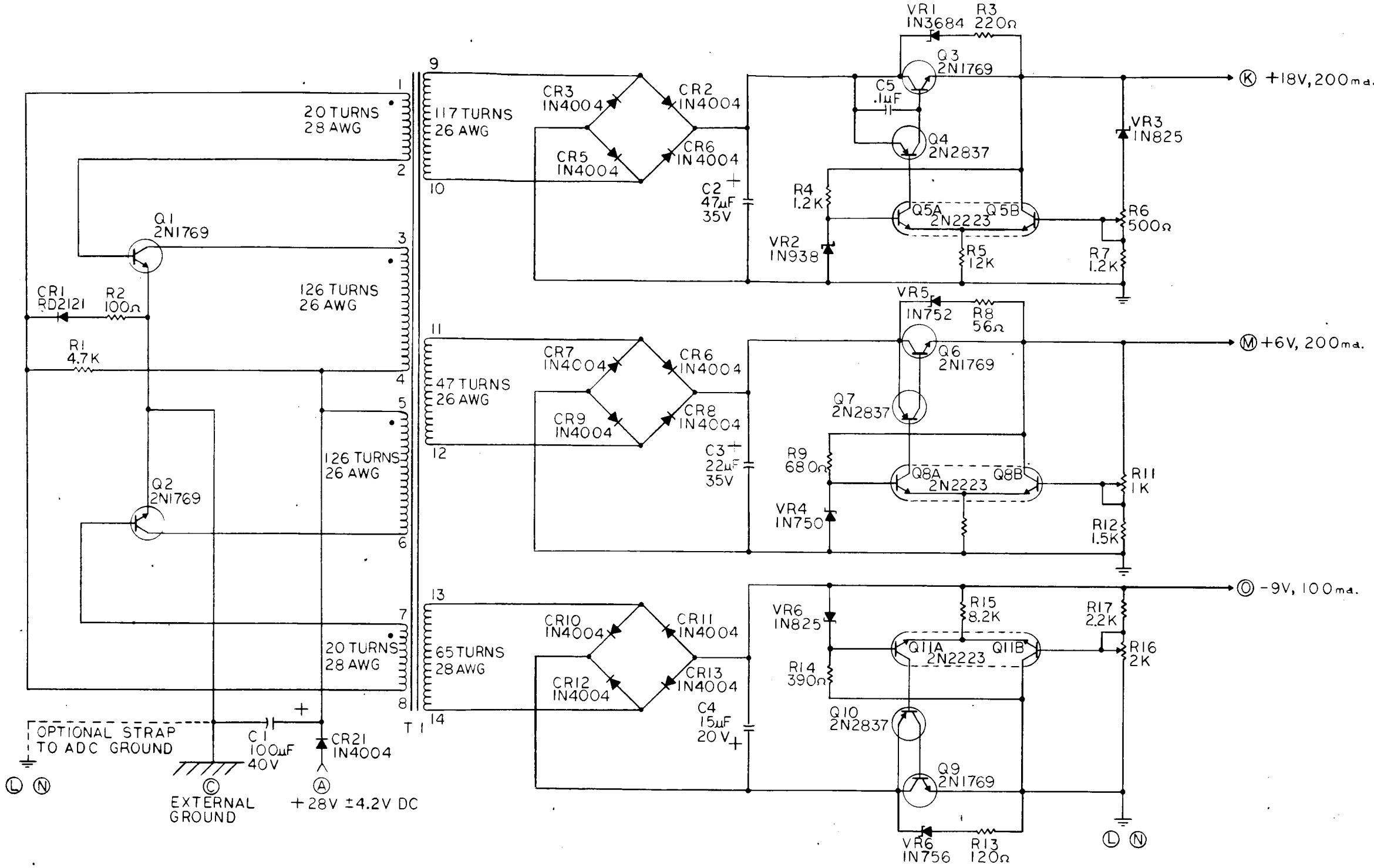
   PRINTED WIRING ASSEMBLY M5559A
2. ASTERISK COMPONENTS MAY BE SELECTED OR OMITTED NOMINAL VALUES MAY BE SHOWN. (SEE ASSEMBLY DRAWING)

1. REFERENCE SUPPLY SCHEMATIC
   M5559A

FIGURE 1



NOTE:

1. REFERENCE DRAWINGS
   PRINTED WIRING BOARD M5560A
   PRINTED WIRING ASSEMBLY M5560A

POWER SUPPLY SCHEMATIC
MB1057-1/M5560A

FIGURE